IN THE CLAIMS

1. (currently amended) A method for operating a flash memory comprising:
programming a memory array with an alternating bit line stress program;
selectively coupling odd local bit lines to odd global bit lines;
selectively coupling even local bit lines to even global bit lines;
determining a logic state pattern of global bit lines in response to the alternating bit line stress program;
comparing the logic state pattern with a predetermined test pattern; and
locating local and global bit line shorts in response to the comparing.

2. (original) The method of claim 1 wherein locating local and global bit line shorts includes indicating a short when a global bit line logic state is an inverse state of what was programmed by the alternating bit line stress program.

3. (original) The method of claim 1 wherein programming the memory array with alternating bit line stress program comprises:
programming even columns of addresses of the memory array to a first logic state; and
programming odd columns of addresses of the memory array to a second logic state that is inverse of the first logic state.

4. (original) The method of claim 3 wherein the predetermined test pattern comprises alternating logic high and low states.

5. (original) The method of claim 4 wherein the memory array is a floating gate memory array and the alternating logical high and low states are comprised of a charge and a lack of charge on the floating gate.

6. (currently amended) A method for operating a flash memory having even and odd local bit lines and even and odd global bit lines, the method comprising:
programming a memory array with alternating logic states;
selectively coupling odd local bit lines to odd global bit lines;

selectively coupling even local bit lines to even global bit lines;

monitoring the global bit lines for a logic state pattern in response to the programming;

comparing the logic state pattern with a predetermined test pattern; and

locating local and global bit line shorts in response to the comparing.

7. (canceled)

8. (currently amended) The method of claim ~~7~~ 1 wherein select transistors are coupled between the local bit lines and the global bit lines.

9. (currently amended) The method of claim ~~7~~ 1 wherein selectively coupling odd local bit lines comprises coupling a first group of alternating local bit lines to a first global bit line and selectively coupling even local bit lines comprises coupling a second group of alternating local bit lines to a second global bit line.

10. (currently amended) The method of claim ~~7~~ 1 wherein selectively coupling odd local bit lines comprises activating a first select transistor that is coupled between a first even local bit line and a first even global bit line.

11. (currently amended) The method of claim ~~7~~ 1 wherein selectively coupling comprises:

generating an activation signal coupled to a control gate of a select transistor; and

the select transistor coupling a first even local bit line to a first even global bit line in response to the activation signal.

12. (currently amended) The method of claim ~~7~~ 1 wherein selectively coupling comprises:

generating a plurality of activation signals, each signal coupled to a different select transistor of a plurality of select transistors; and

the plurality of select transistors selectively coupling the even local bit lines to the even global bit lines and the odd local bit lines to the odd global bit lines in response to the activation signals.

13. (currently amended) The method of claim ~~7~~ 1 wherein the integrated circuit memory is a flash memory device.

14. (currently amended) A method for operating a flash memory having even and odd local bit lines and even and odd global bit lines, the method comprising:
programming a plurality of memory cells of a memory array with alternating logic states;
selectively coupling odd local bit lines to odd global bit lines;
selectively coupling even local bit lines to even global bit lines;
monitoring the global bit lines for a logic state pattern in response to the programming;
comparing the logic state pattern with a predetermined test pattern; and
locating local and global bit line shorts in response to the comparing.

15. (original) The method of claim 14 and further including indicating a short when a global bit line logic state is an inverse state of what was programmed into an associated memory cell of the plurality of memory cells.